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AERONAUTICAL RESEARCH LABORATORY

MELBOURNE, VICTORIA

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Flight Mechanics Technical Memorandum 422

A MICROPROCESSOR CONTROLLED STRAIN GAUGE CALIBRATION MODULE

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by

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C.W. Sutton
and
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SUMMARY

This report describes the electronics module which interfaces the recently developed strain gauge balance calibrating machine with the ARL low speed wind tunnel data acquisition and control computer system.

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1. INTRODUCTION

The traditional method of calibrating multi-component wind tunnel strain gauge force balances involved the application of forces, singly and in combinations, using weights and appropriate mechanisms. Normally the balance and loads had to be re-aligned for each load increment. This method involved arduous physical work and was very time consuming.

A new method has been developed at ARL which involves comparing the balance to be calibrated to a precision master balance. The balance to be calibrated and the master balance are so arranged that their calibration axes are coincident and no re-alignment is required during the calibration process.

Loads are applied by pneumatic cylinders which will ultimately be computer controlled. This avoids the extensive weight handling previously required. It is expected that the new calibration system will reduce the time required for a complete second order calibration of a six-component balance from weeks to hours.

2. SYSTEM DESCRIPTION

2.1 Strain Gauge Calibration (SGC) Module)

The SGC module contains a 68000 microprocessor and is compatible with the distributed intelligent data acquisition system which links to the dedicated computer of the subsonic wind tunnel (Ref.2).

The SGC module was developed to interface the master balance load cell outputs and the outputs of the balance being calibrated.

Extensive use has been made of in-house developed card sets and high performance amplifiers.

The SGC module (Fig. 1 & 2) contains twelve strain gauge amplifiers of which six are precision D.C. amplifiers permanently connected to the load cells of the calibration rig. The other six strain gauge amplifiers may be precision D.C. amplifiers but are generally high performance self-balancing A.C. amplifiers that connect to the strain gauge bridges of the balance undergoing calibration. Construction of the amplifiers is shown in Figures 3 and 4.

Under microprocessor control, and within the SGC module, are six dual analogue to digital converter cards, which provide twelve channels of 16 bit binary readings that relate to the output signals from the strain gauge amplifiers.

The large thermal mass of the temperature compensated load cells allows D.C. excitation at five or ten volts, but the self-heating of small multicomponent and control surface strain gauge balances is minimised by using one volt A.C. excitation.

Typically, the SGC module connects to the host computer through either a parallel bus or a serial port. A second serial port is available for connection to an operator's Teletypewriter terminal. During set-up and pre-calibration stages the SGC module may be disconnected from the host and hard copy printout obtained from the operator's terminal located near the calibration rig.

The microprocessor resident program (within the SGC module) accepts command codes from the host to control channel selection and trigger readings. Selected data from the balance and load cell channels, with error messages, are sent to the host and/or the terminal.

2.2 The Calibration Rig

The rig which is basically a precision six component strain gauge balance is shown in Fig. 5. The balance to be calibrated is mounted by its "live" attachment point to the floating frame (F). A series of flexure pivoted push rods and precision load cells (M) transfer the applied loads to an earth frame (E) which is kinematically mounted from a support frame (S).

Calibration loads are applied between the supporting structure and the "earth" end of the balance under calibration using six pneumatic cylinders (Fig. 6). Control of the pneumatic loads applied is provided by separate adjustable pressure regulators for each cylinder.

Solenoid operated valves, currently under manual control, set the loads but microprocessor capability exists for future automatic load control. The resulting force and moment signals from the strain gauge balance and the load cell channels are measured by the SGC module for processing by the host computer.

3. STRAIN GAUGE INSTRUMENTATION

3.1 General

Wiring between the SGC module and the calibration rig supports remote sensing of the excitation supply through the six wire bridge concept.

Each amplifier contains a calibration resistor, which may be switched across a bridge arm by contacts of a reed relay, to readily perform a channel calibration check. This function is initiated by software commands from the host.

Voltage comparators within each amplifier trigger an "overload" timer whenever a peak signal exceeds the preset voltage signal limit for the input stage. The timer signal initiates an "overload" error message. The timer remains latched for a minimum of five seconds after removal of the overload signal to guard against nonlinearity errors within the amplifier stages.

3.2 D.C. Precision Amplifiers

A block diagram of a D.C. amplifier is shown in Fig. 7. Each D.C. excitation supply is derived individually, within the amplifier chassis assigned to that channel, by a remote sensing precision voltage regulator. An internal switch provides for an output excitation of either five or ten volts. A Metal Oxide Semiconductor Field Effect Transistor (MOSFET) provides the current capacity to drive a 120 ohm load.

Zero balance is provided by a ten turn potentiometer and the switched gains of X30, X100, X300 and X1000 are screwdriver selectable from the front panel. The balance must be readjusted whenever a gain change is made. But, in general, the gain setting need not be changed during calibration as even at 10% of full scale a 0.1% resolution is obtained because of the 0.01% full scale accuracy of the system.

3.2.1 Excitation stability

Stability with load (24 degrees C.)

LOAD (ohms)	EXCITATION (Volts)	
	5	10
5000	4.9947	10.0044
120	4.9947	10.0044

Stability with time (120 ohms across 5 volt supply)

0.001 %/hour

Stability with temperature (10 to 40 degree C.)

0.001 %/degree C.

3.2.2 Gain and offset

Absolute amplifier gains are within +/-0.2% of the nominal X30, X100, X300, X1000 values.

Gain stability (X1000, filter 0.6 Hz)

with temperature	0.006%/degree C.
with time	0.003%/hour

Input offset

with temperature	0.07 microvolts/degree C
with time	0.4 microvolts/hour 17 pico amperes/hour

3.2.3 Low pass filters

A front panel screwdriver selectable three-position switch selects two pole low-pass Butterworth filters with -3 db at 0.6 Hz and 1 kHz respectively. Typically, the frequency response in the 25 kHz position (filters out) is 27 kHz.

3.3 Self-balancing A.C. Amplifiers

The principle of the self-balancing A.C. amplifier is contained in References 3 & 4. *A simplified block diagram is shown in Fig.8.*

The full scale output signal is +/- 10 volts for an input of between +/-400 microvolts to +/- 6 millivolts. For a full four gauge bridge this 15:1 gain ratio corresponds to a range of between +/-200 microstrains to +/-3000 microstrains.

Amplifier linearity is typically better than 0.01%. Drifts, referred to the input at the highest gain setting, are:

200 nanovolts/day
10 nanovolts/degree C.

The overload detector ahead of the low-pass filter senses for front end signal overload to initiate an "overload" (Section 4.1.3) and illuminates a front panel indicator. The overload detector trips at a voltage level 10% beyond full scale limits and latches for a minimum of five seconds. Although such overloads are unlikely during calibration, identical amplifiers are used in the wind tunnel data acquisition system where dynamic forces and moments are often encountered by the model.

3.3.1 Excitation Supply

A single A.C. excitation bridge supply is provided on a card within the SGC module, to power the six strain gauge bridges of the balance under calibration. The excitation supply, generated digitally (Fig. 9), has excellent amplitude and frequency stability with low distortion.

Three binary counters (Fig.10), pre-loaded with hex. value 7CF (decimal 1999), are clocked at two MHz. Every millisecond the counter clocks down to zero and the reset logic reloads the counters. Eleven of the twelve lines from the counters address a 2K x 8 bit EPROM which currently provides 2000 discrete eight bit parallel codes to a digital to analogue converter.

The EPROM contains a sine function in increments of 0.18 degrees over a range of 0 to 360 degrees with the option of smaller increments. Incrementing, over a reduced range of 180 or 90 deg, is also possible but incurs greater circuit complexity.

The 1kHz sinusoidal crystal controlled output from the digital to analogue converter is buffered by operational amplifiers and drives a ferrite pot-core transformer. The secondary voltage of the transformer provides a one volt RMS output to the strain gauge bridges.

Rectified feedback from the transformer to the Vref pin of the converter was contemplated, but was unnecessary.

Stability with load

LOAD (ohms)	RMS OUTPUT (volts)
120	1.001
20	1.000
15	0.998
10	0.997

3.3.2 S.G. Amplifier Input Arrangements

Each amplifier, whether AC or DC type, is constructed as a plug-in module using cassettes to VME single height standard. The plug-in connection is made with a 96 pin DIN41612 connector carrying power supply, signal and all other input and output lines. This provides compatibility among the 12 channels so that the pin list for each channel is identical.

A wiring loom using screened leads for each channel input and drive signals makes the connection from the amplifiers to the S G C module input sockets.

The external cabling from the load cells and balance terminates at the SGC module end with 64 pin DIN41612 connectors; one for the DC amplifiers (SK 1 channels 1-6) and another for the AC amplifiers (SK 2 channels 7-12).

Pin details for these two sockets are listed in APPENDIX 1.

3.4 Software Controlled Calibration Check

A software controlled calibration check for the analogue channels has been included in the SGC module. The circuit boards of both A.C. and D.C. amplifiers include a relay which is energised by an external source to unbalance the sensing bridge circuit by placing a precision resistor of selected value across one arm.

Connections to the relay are identical at the P.C.B. connector of the A.C. or D.C. amplifier maintaining compatibility between modules.

A relay drive card which connects to the VME bus is addressed by the host to operate or release the relay using one address only. The data bus contains the information to cause the logic circuit on the drive board to activate or de-activate the relay coil voltage. The card is addressed as FFAEF7, with the hexadecimal codes OC to calibrate and 03 to cancel.

The keyboard command to invoke the calibration resistor is "@". Any other key will disable the calibration function.

3.5 Dual Analogue to Digital Converter Card

Fig.11 shows a block diagram of the dual 16 bit analogue to digital converter and the finished multiwire card is shown in Figure 12. Each card is assigned three addresses. One address is common to all cards and, when written to by the microprocessor, initiates a simultaneous start conversion for all cards. Each channel of the dual card is assigned a unique address. A write to either address starts the simultaneous conversion for both channels on the card. Individual channel data is read by the microprocessor addressing one of the two unique addresses.

COMMON CONVERSION ADDRESS OFFE600

CARD	CHANNEL	ADDRESS
1	1	OFFE610
1	2	OFFE620
Through to		
6	11	OFFE6BO
6	12	OFFE6CO

The analogue signal passes through a differential amplifier and second order low-pass filter to a sample and hold stage. The analogue signal input impedance is greater than 50K ohms and the common mode rejection ratio is better than 106 decibels at 100 Hz. The low pass filter has a cut-off of -3db at 20 Hz and the droop rate of the sample and hold during conversion is a few microvolts. Typically, drift is +/- 2 bits/day and a temperature change of 5 degrees C. produces a 1 bit change.

Conversion requires about 50 microseconds and the 16 bit parallel output corresponds to an analogue input range of +/- 10 volts. Thus the least significant bit represents 0.0015% (1 in 65535 of full scale or 305 microvolts).

4. MICROPROCESSOR CONTROL

4.1 Communication

Data, transmitted to the operator's terminal, are scaled in signed decimal voltage with six values/line. Thus the twelve available channels are displayed as two lines of data with the load cell channels on the first line and the strain gauge balance channels on the second line.

Single line error messages may also appear on the terminal (Section 4.1.3). The choice of terminal is important and (unless of a hard copy variety) cursor control is required since:

(1) The two data lines need to be overwritten by new data to remain stationary on a visual terminal, otherwise the display scrolls upwards and viewing is difficult.

(2) The single line message(s) need to be erased prior to display of new data otherwise residue characters from cancelled error messages remain displayed.

Fast reading rates are not essential for the calibration application but a time penalty is incurred to erase a video screen or to selectively overwrite message lines with spaces. Currently, data are not buffered and serial transmission to the terminal slows the reading rate. However, buffering or selective sampling of data for display could be implemented with slight changes to the microprocessor resident control program.

Transmission to the operator's terminal is therefore formatted for viewing and currently a Teletypewriter for hard copy output is assumed (Fig.13). Serial communication to the host and terminal involves stringed ASCII characters. However, faster reading rates require 16 bit parallel communication with the host.

A three position toggle switch, located on the panel of the opto-isolator card (Section 4.3) causes the resident program of the SGC module to branch, following reset or power-on, to support:

(1) Serial operation with host
(2) Parallel operation with host (future facility)
(3) Monitor interrogation of SGC module with terminal

The host (or substituted terminal) provides the codes (Figs 14 and 15) to control the SGC module as detailed in Section 4.1.4. The operator terminal, when connected, has only the capability to prompt the next set of readings and control the calibration relay.

4.1.1 Serial

Dual RS-232 serial ports provide optional connection of the SGC module to the operator's terminal and/or host.

UPPER PORT: 300 baud, even parity, 7 data bits, 2 stop bits. (corresponds to KSR43 with all three top right switches "UP")

LOWER PORT: 4800 baud, no parity, 8 data bits, 1 stop bit.

4.1.2 Parallel

Provision exists to accept the parallel (16 bit) instrumentation bus which uses a daisy chained twisted pair ribbon cable. RS-485 type differential driver/receivers at the host end of the cable handshake with those residing on a parallel communication card installed in the SGC module.

4.2 Error Codes and Messages

Detection of an error by the SGC module causes transmission of a symbol to the host or an appropriate error message to the terminal.

Currently, the conditions that produce a response are:

missing data	Question marks are substituted for the missing data characters. Also the single line message "missing readings from channels n1, n2" is sent to the terminal.
non selected channels	Spaces are substituted for the non selected channel data.
channel data overrange	The single line message "overload on channels n1; n2;" is sent to the terminal. A dollar ($) is substituted for the leading space associated with overranged data sent to the host.

NOTES:

(1)	The sign of the data identifies the direction of overrange.
(2)	To avoid visual confusion when a $ is displayed between two data values, apply the money convention of the $ preceding the value.
amplifier overload	As for channel data overrange (Section 3.3)
A.C. excitation	The single line message "strain gauge excitation level error" is sent to the terminal. Character string "SGLO" proceeds the data string sent to the host.
time out	The single line message "time out NIL readings" is sent to the terminal. Character string "TIME" is sent to the host.

4.3 Host Command

Command facilities currently available for host control of the SGC module uses single ASCII printable characters to avoid possible conflict with host interface operation through the use of non-printable control characters within the range 00 to 1F (hexidecimal). The command functions are detailed in Figs. 14 and 15.

The command function is determined by the logic state of bit 6 of the ASCII character received through the lower serial port or through the parallel bus port.

If bit 6 is a logic 1 then the character implements a change to the channel selection code.

If bit 6 is a logic 0 then the character implements a change to the mode control code.

4.3.1 Channel selection

The default setting for the channel selection code is for all 12 channels to be "selected"; thus bit 0 through to bit 11 (Fig 14) are initially set to a logic 1 state. The channel selection code is changed in blocks of four channels whenever a host character is detected with bit 6 at a logic 1.

The first block, representing channels 1 to 4, is changed if bits 4 and 5 of the character are at logic 0. As tabulated in Fig 15, a range of 16 printable ASCII characters (@ to 0 representing the hexadecimal range 40 to 4F) can therefore cover all the possible combinations of channel selection within the first block. Similarly, the second block, representing selection of channels 5 to 8, is changed if the character has bit 4 a logic 1 and bit 5 a logic 0. Likewise, the selection code for channels 9 to 12 changes if bit 4 is a logic 0 and bit 5 is a logic 0.

The change in the channel selection code is produced by the four low order bits of the character replacing the 4 bits in the assigned block. Thus any bit pattern for the channel selection code is achieved with three or less specific character commands.

4.3.2 Mode control

Provided the character byte has bit 6 at a logic 0 and bit 5 at logic 1 then the logic state of bit 4 determines which half of the eight bit wide mode control code is replaced by the four low order bits of the character byte. If bit 4 of the character byte is a logic 0 then bits 0 to 3, in the mode control code, are changed; otherwise the change relates to bits 4 to 7.

4.4 Operator terminal command

Communication with the operator terminal through the upper serial port does not support command options except that any single key stroke at the terminal initiates a single set of readings.

Successive keying of an @ character (requires the use of the shift key on the Model KSR 43 Teletypewriter terminal) initiates single sets of readings with alternative connection of the calibration resistors (Section 3.4).

4.5 Opto-isolator Card

The opto-isolator card (Fig. 16) has the capacity to accept up to sixteen inputs. Current flow through the light emitter portion of the isolator produces a logic high at the respective bit of the output word.

The opto-isolator card is assigned the address OFFAEEO for access by the SGC module microprocessor and "dtack" is returned within 200 nanoseconds.

Twelve inputs are allocated to the twelve strain gauge amplifier channels for detection of amplifier overloads. Another input senses the A.C. strain gauge excitation voltage, and two more inputs sense the state of the three position toggle switch used to select serial, parallel or monitor mode (Section 4.1) for the SGC module resident program. Bit allocation is shown in Fig.17.

On the positive edge of an input change the opto-isolator card is able to initiate a level 1 (lowest priority) interrupt to the microprocessor, with an interrupt vector of 70.

For input changes to be recognised, the change must remain asserted for at least one system clock period (62.5 nanoseconds).

5. MODULE HARDWARE

The SGC module is of double height double depth construction to accommodate two rows of six amplifiers along the front of the module. The wiring is arranged with the load cell channels allocated to the upper six amplifiers (channels 1 to 6) and the strain gauge balance (channels 7 to 12) to the lower six amplifiers. Front view channel numbers run from left to right (Fig. 18a).

All plug-in cards are single-height and are accessed from the rear of the module (Fig.18b). The microprocessor back plane contains 19 slots and occupies the upper rear portion of the module while a switched power supply unit and fan occupy the lower rear portion of the module.

All cards and strain gauge amplifiers are constructed to Eurocard standards. The microprocessor backplane is VME compatible and the module hardware is constructed from standard Eurocard components.

The one major departure from orthodox construction is that the double depth chassis has side plate hinges to allow easy access to the back-to-back connector wiring located along the center plane of the module. The side plate join is visible in Figures 1&2.

6. OPERATING INSTRUCTIONS

1. Ensure that the load cells and the strain gauge balance leads are properly connected and conform to the pin allocation given in APPENDIX 1.

   NOTE: Channels 1 to 6 represent the D.C. amplifiers and should connect to the load cells.

   Channels 7 to 12 represent the A.C. amplifiers and should connect to the strain gauge balance.

2. For SERIAL communication ensure that the three position switch, located on the rear panel of the opto-isolator card (Fig. 16) is in the "SER" position and:

   a. The upper port connector on the dual serial card (Fig. 18b) connects to a KSR43 Teletypewriter (or equivalent) for the hard copy print out of messages and readings, scaled in signed decimal voltages, for the operator.

   b. The Teletypewriter should be placed near the Strain Gauge Calibration Rig, since a key press prompts the next reading.

   c. The lower port connector on the dual serial card (Fig. 18b) connects to the host computer or a visual display unit. Readings transmitted through the lower port are in hexadecimal code and combine with error symbols as detailed in Fig. 15.

The lower port accepts commands to control the selection of channels and mode of operation as defined in Figs. 14 and 15.

NOTE: for serial operation of the SEC module, either or both ports of the dual serial card must be connected as described above otherwise readings cannot be prompted or recorded (except by parallel communication with the host).

3. For parallel communication ensure that the three position switch, located on the opto-isolator card (Fig. 16), is in the "PAR" position and:

   a. The woven ribbon cable of the differential bus from the host connects to the parallel communication card.

   NOTE: In either the serial or parallel mode, only the host has total control of the SGC module through the commands detailed in Figs 14 and 15.

4. Apply mains power and with rear located MAINS switch "ON" check that the fan functions and that all the "PWR ON" indicators fitted to the front panels of the amplifiers are illuminated.

5. The "OVERLOAD" indicators should extinguish on all amplifiers within 10 seconds.

6. Check, and if necessary change, the settings of the slotted shaft switches associated with the gain and low-pass filter of each amplifier; prompt readings and zero adjust the channels using the "ZERO" controls with the pneumatic loads off; initiate a CAL command and check the validity of the reading.

7. Commence the calibration by applying the first combination of loads and prompt a reading. Repeat until all load combinations have been applied.

8. For MONITOR use place the three position switch on the opto-isolator card to "MON" and:

    a. Ensure that a Teletypewriter or equivalent terminal is connected to the upper port of the dual serial card.

    b. Press the rear "RESET" switch (Fig 18b).

    c. Type "H" for help on the terminal keyboard to obtain the current facilities, in menu form, available for interrogation of the SGC module (Fig.13).

ACKNOWLEDGEMENTS

The authors wish to thank N. Pollock and B.D. Fairlie for raising the Task to develop the strain gauge calibration module. Construction and assembly of the module was shared between T.S. Stanford and I.M. Kerton; A.J. Leslie assembled, tested and calibrated the analogue to digital cards and R.J. Anderson was involved in the assembly and performance testing of the D.C. precision amplifiers.

I.G. Powlesland contributed to the VME card development, initial design and testing of the D.C. strain gauge amplifier prototype and with special module construction methods.

The A.C. self-balancing amplifiers were built commercially, to the design of N. Pollock, and the digitally generated A.C. excitation supply was the concept of G.W. Burnett.

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APPENDIX 1

STRAIN GAUGE CALIBRATION MODULE
AMPLIFIER INPUT CONNECTIONS

DC Amplifiers: Input socket pinlist (SK 1)

AMP. No.	SOCKET	I/P −	I/P +	SENSE −	SENSE −	EXCIT. −	EXCIT. +
1	SK9	5c	4c	6a	3a	6c	3c
2	SK10	10c	9c	11a	8a	11c	8c
3	SK11	15c	14c	16a	13a	16c	13c
4	SK12	20c	19c	21a	18a	21c	18c
5	SK13	25c	24c	26a	23a	26c	23c
6	SK14	30c	29c	31a	28a	31c	28c

AC Amplifiers Input socket pinlist (SK 2

AMP.No.	SOCKET	INPUT		SENSE		EXCIT.		REBAL.
7	SK3	5c	4c	3a	6a	6c	3c	5a
8	SK4	10c	9c	8a	11a	11c	8c	10a
9	SK5	15c	14c	13a	16a	16c	13c	15a
10	SK6	20c	19c	18a	21a	21c	18c	20a
11	SK7	25c	24c	23a	26a	26c	23c	25a
12	SK8	30c	29c	28a	31a	31c	28c	30a

APPENDIX 2

SK 1, SK 2 SOCKET DETAILS
(DC Polarities shown apply to DC amp. inputs only)

	a	c	
	32	32	
6 sense-	31	31	-excit 6
6 rebal	30	30	-input 6
	29	29	+input 6
6 sense+	28	28	+excit 6
---------	27	27	------------
5 sense-	26	26	-excit 5
5 rebal	25	25	-input 5
	24	24	+input 5
5 sense+	23	23	+excit 5
---------	22	22	------------
4 sense-	21	21	-excit 4
4 rebal	20	20	-input 4
	19	19	+input 4
4 sense+	18	18	+excit 4
---------	17	17	------------
3 sense-	16	16	-excit 3
3 rebal	15	15	-input 3
	14	14	+input 3
3 sense+	13	13	+excit 3
---------	12	12	------------
2 sense-	11	11	-excit 2
2 rebal	10	10	-input 2
	9	9	+input 2
2 sense+	8	8	+excit 2
---------	7	7	------------
1 sense-	6	6	-excit 1
1 rebal	5	5	-input 1
	4	4	+input 1
1 sense+	3	3	+excit 1
	2	2	
	1	1	

Front view of pinout of DIN 41612 sockets SK1,SK2

AC amplifiers follow the same sequential grouping, ie ch7 to 12 emulate the layout above for ch1 to 6 respectively

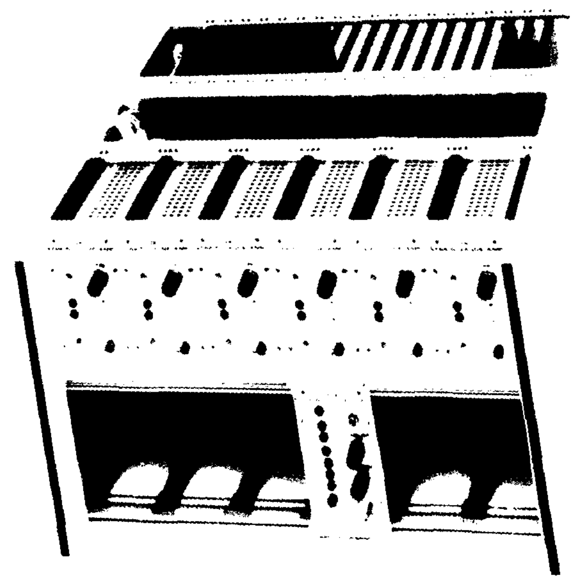


FIG. 1 FRONT VIEW OF S.G.C. MODULE

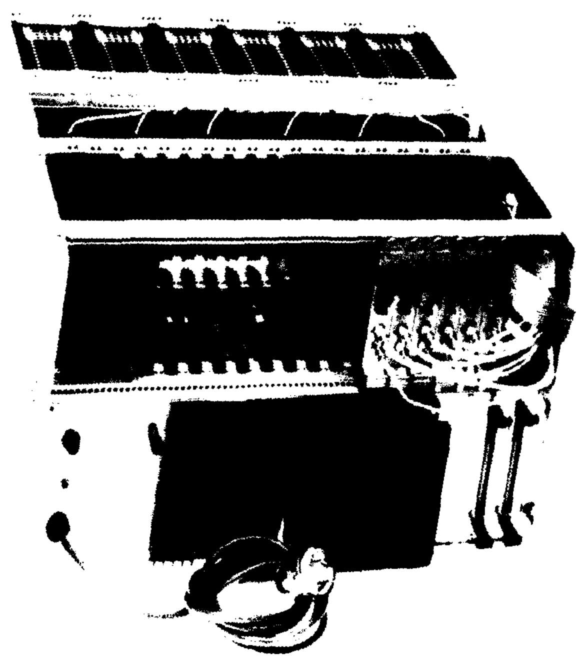


FIG. 2 REAR VIEW OF S.G.C. MODULE

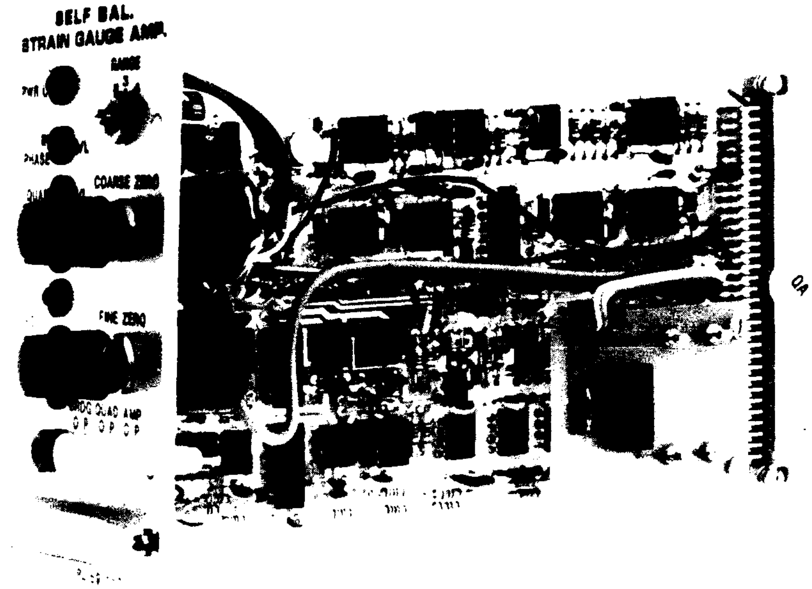


FIG. 3 SELF-BALANCING A.C. STRAIN GAUGE AMPLIFIER

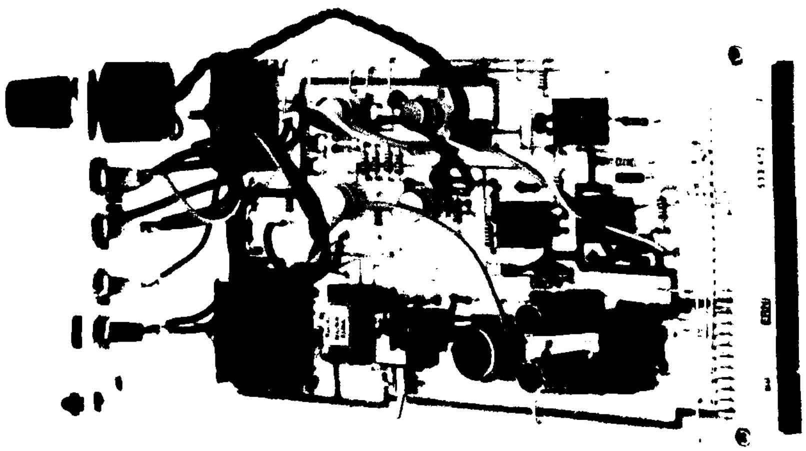
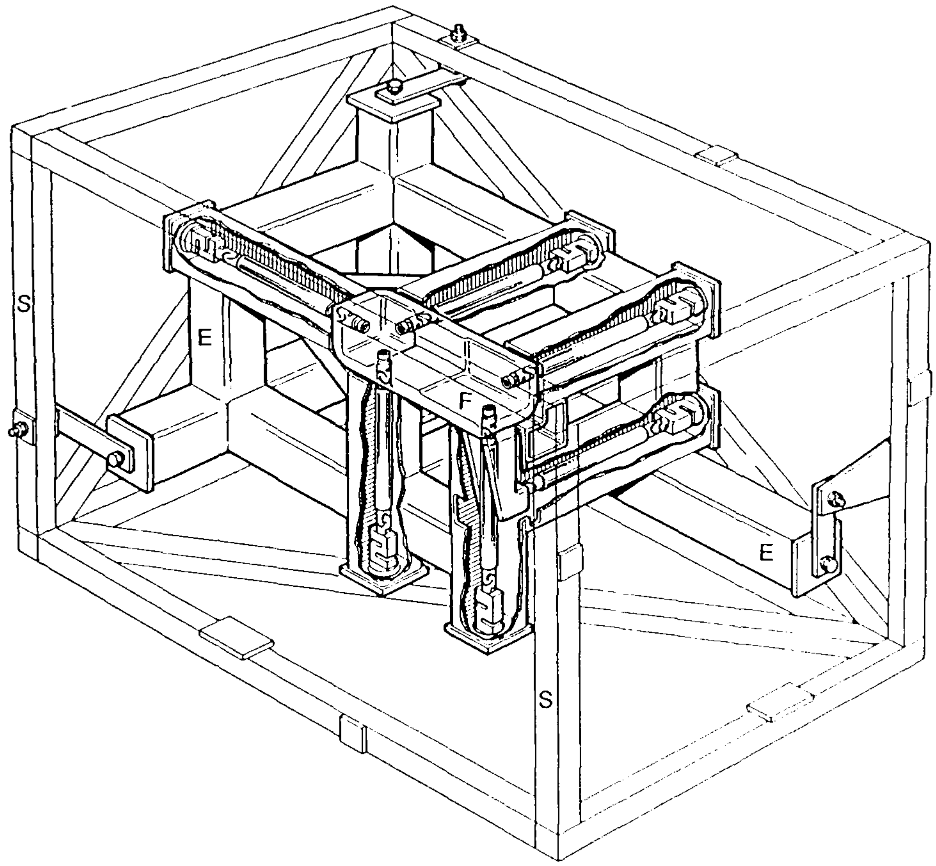
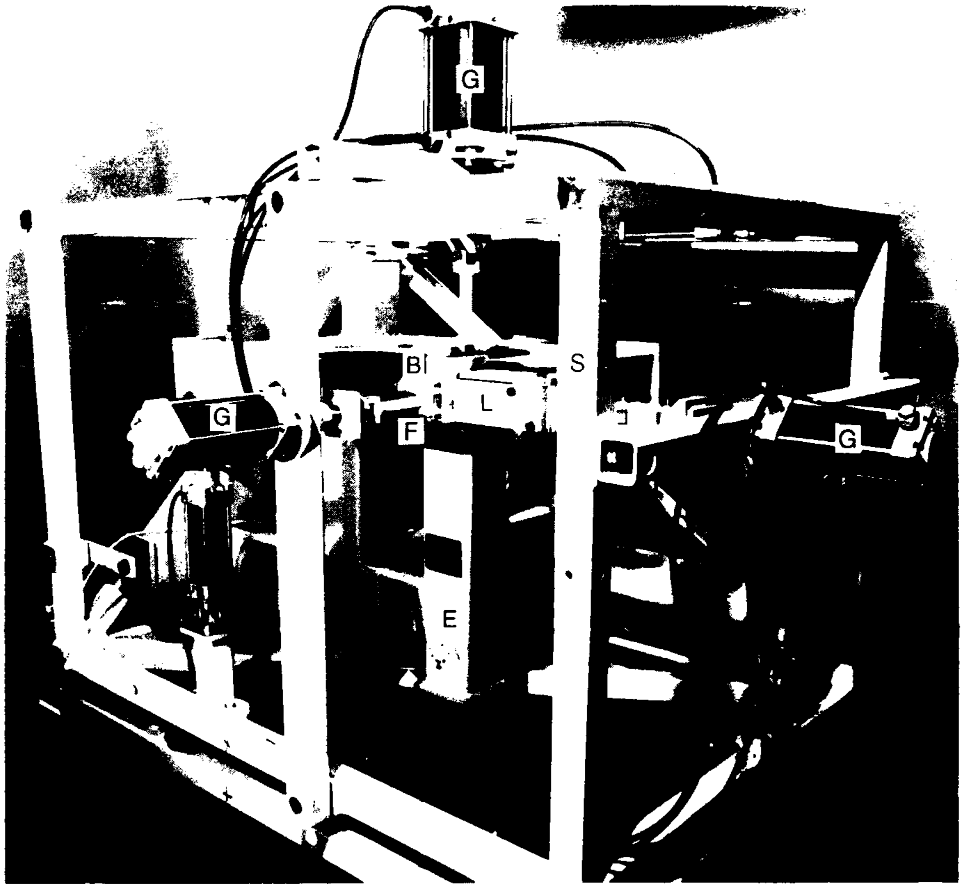


FIG. 4 PRECISION D.C. STRAIN GAUGE AMPLIFIER



E. Earth frame
F. Floating frame
M. Master balance
S. Supporting structure

FIG. 5. ISOMETRIC VIEW OF MASTER BALANCE AND SUPPORT FRAME



B Balance under calibration
E Earth frame
F Floating frame
G Force generators
L Loading frame
S Supporting structure

FIG. 6 PHOTOGRAPH OF BALANCE CALIBRATING MACHINE

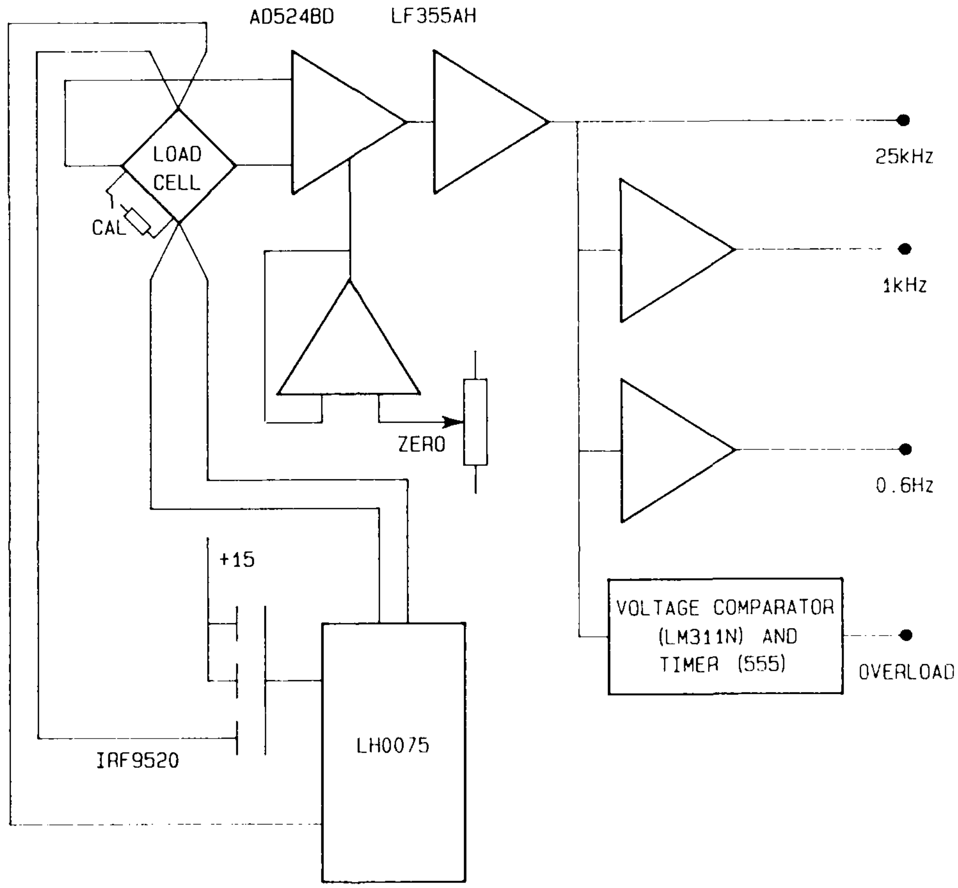


FIG. 7. D.C. PRECISION AMPLIFIER SCHEMATIC

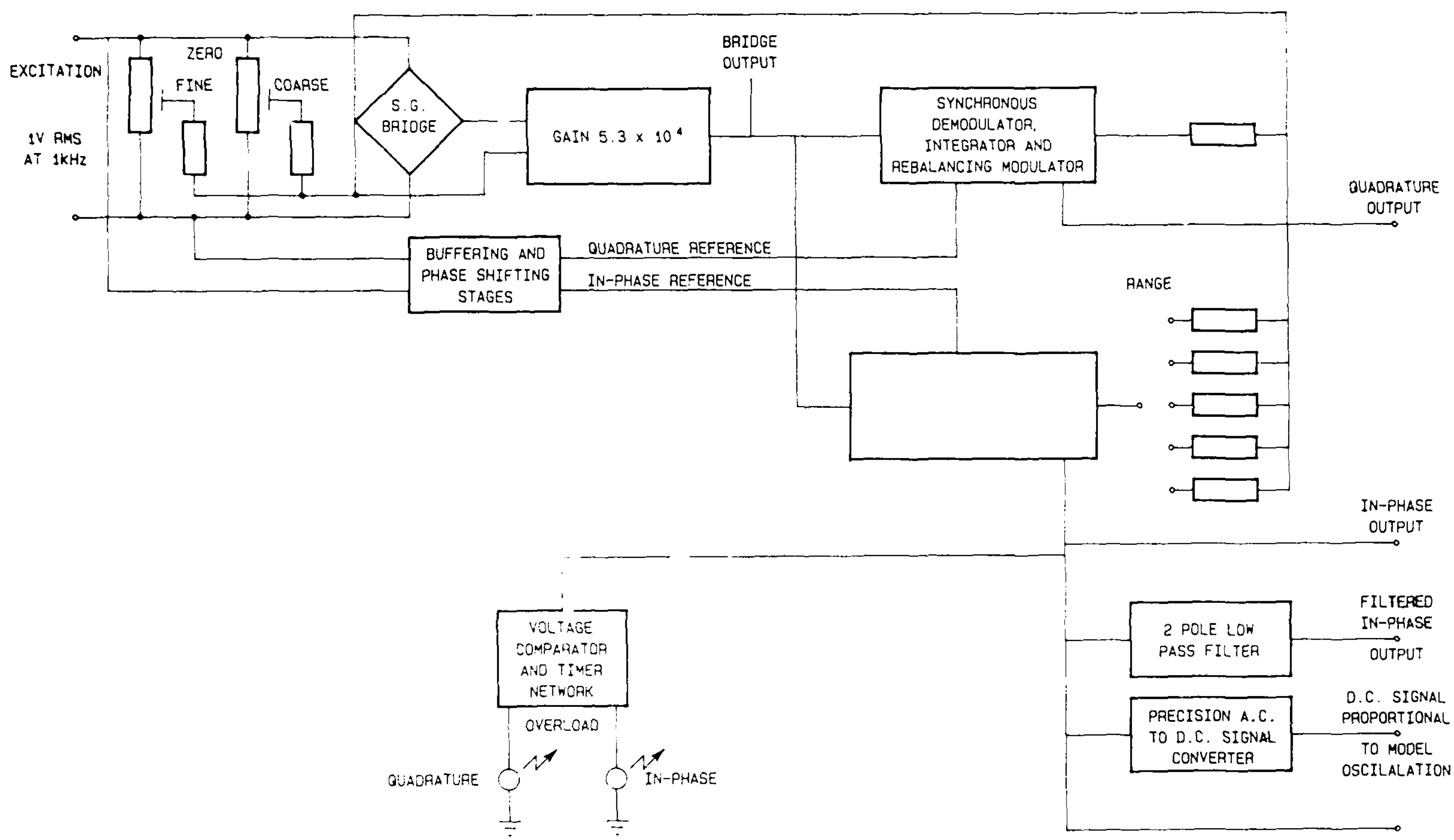


FIG. 8. SIMPLIFIED DIAGRAM OF SELF-BALANCING A.C. AMPLIFIERS

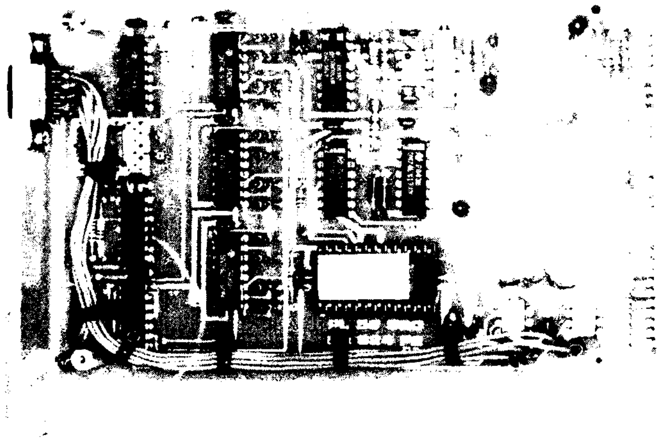


FIG. 9. A.C. EXCITATION BRIDGE SUPPLY CARD

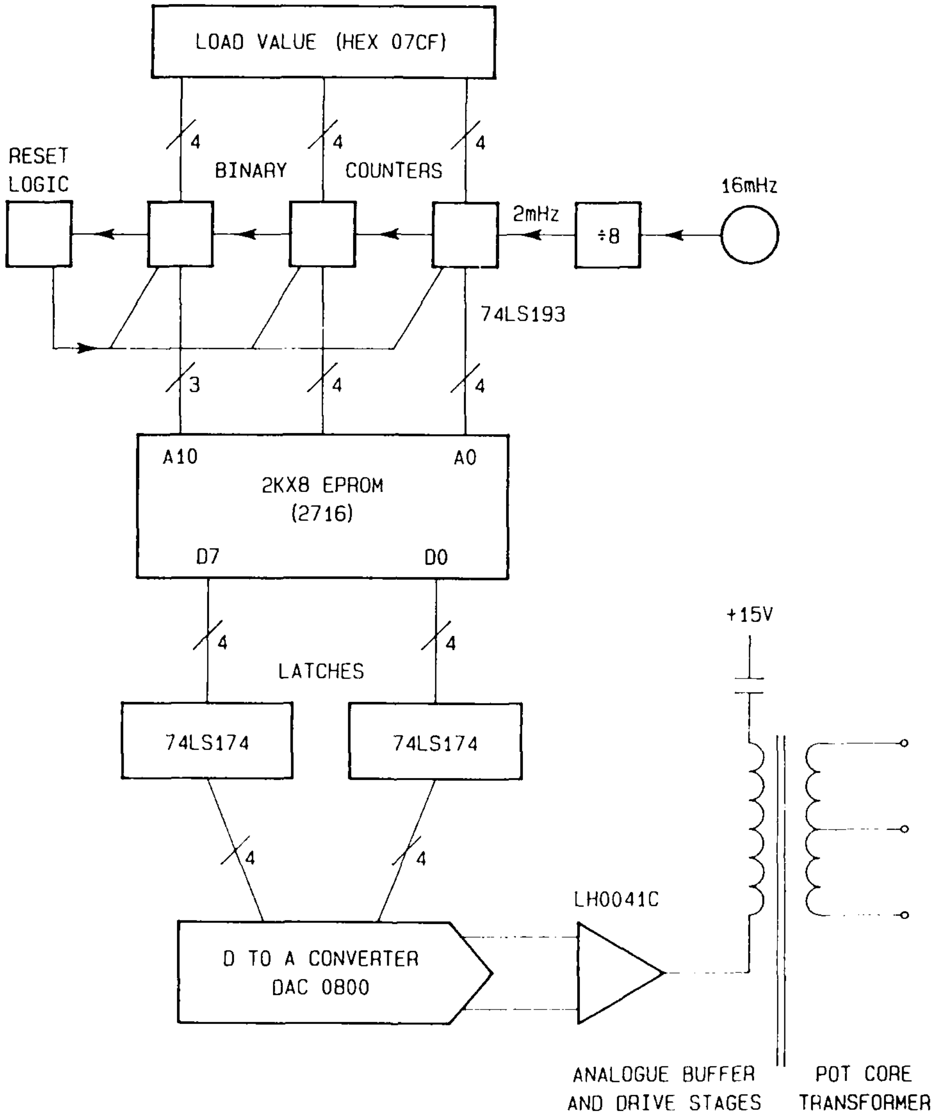


FIG. 10. A.C. EXCITATION BRIDGE SUPPLY

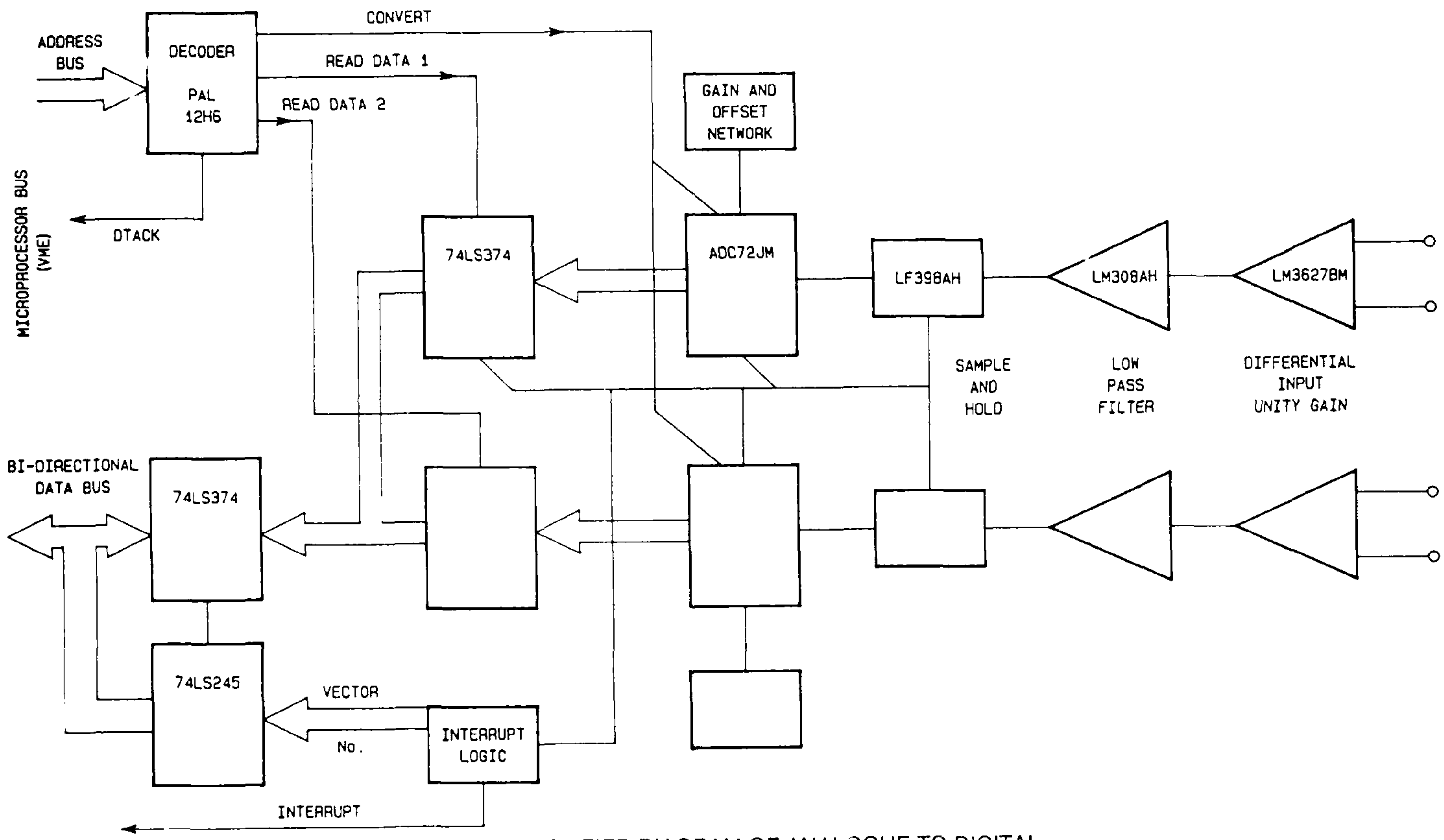


FIG. 11. SIMPLIFIED DIAGRAM OF ANALOGUE TO DIGITAL CONVERTER CARD

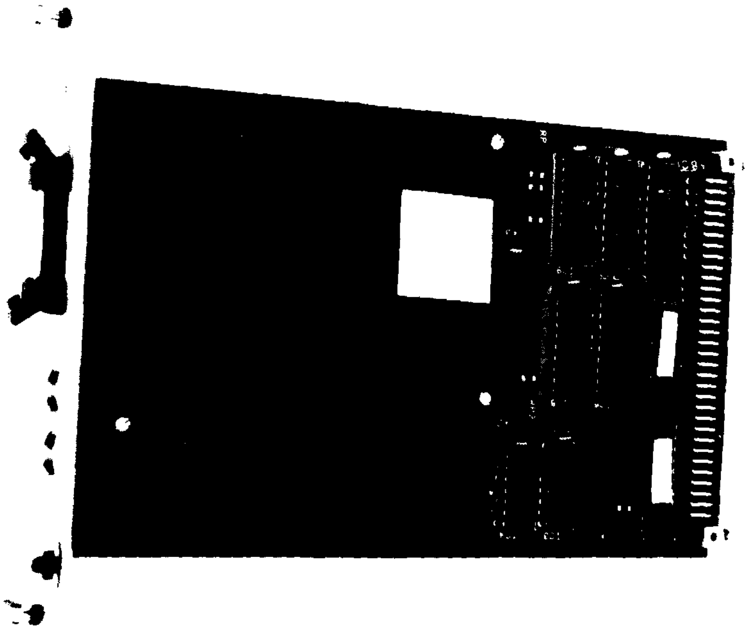


FIG. 12. DUAL ANALOGUE TO DIGITAL CONVERTER CARD WITH SHIELD ATTACHED

68000 MONITOR PROGRAM FOR WIND TUNNEL CALIBRATE MODULE

ARL AERO-IFEG Version 1.3(a) Jan. 1987
(For use with KSR43 terminal)
Type H for help
(Monitor Scratch Pad RAM Hex 4000 4fff)
(User RAM HEX 6000 6fff)

HI! H
A-- Alter data in memory. A space displays next memory location, a return returns to the monitor.
B-- Insert breakpoint at specified address.
C-- Communicates with Host via Port J1.
(To return to ROM monitor Type C)
NOTE: Motorola S Code loaded through PM4422 "sdump".
D-- Display block of data between specified locations.
Comma used as a delimiter.
E-- Error sent from Device Reporting Card.
G-- Executes program from specified address
I-- Inspect status of device report card.
S-- Single steps through program.

STRAIN GAUGE CALIBRATION RIG
ARL AERO-IFEG Serial Ver. 1.3 (KSR43) Jan 1987

OVERLOAD ON CHAN. 04;07;08;09;10;11;12;

+0.7022 +0.0610 -4.2834 -9.9996 -0.0241 -0.0241
+9.9996 +9.9996 +9.9978 +9.9996 +9.9996 +9.9996

OVERLOAD ON CHAN. 04:07;08:09;10;11;12;

+0.7211 +0.0485 -4.2645 -9.9996 -0.0241 -0.0241
+9.9996 +9.9996 +9.9978 +9.9996 +9.9996 +9.9996

FIG. 13 MONITOR AND SIGNED DECIMAL VOLTAGE AT OPERATORS TERMINAL

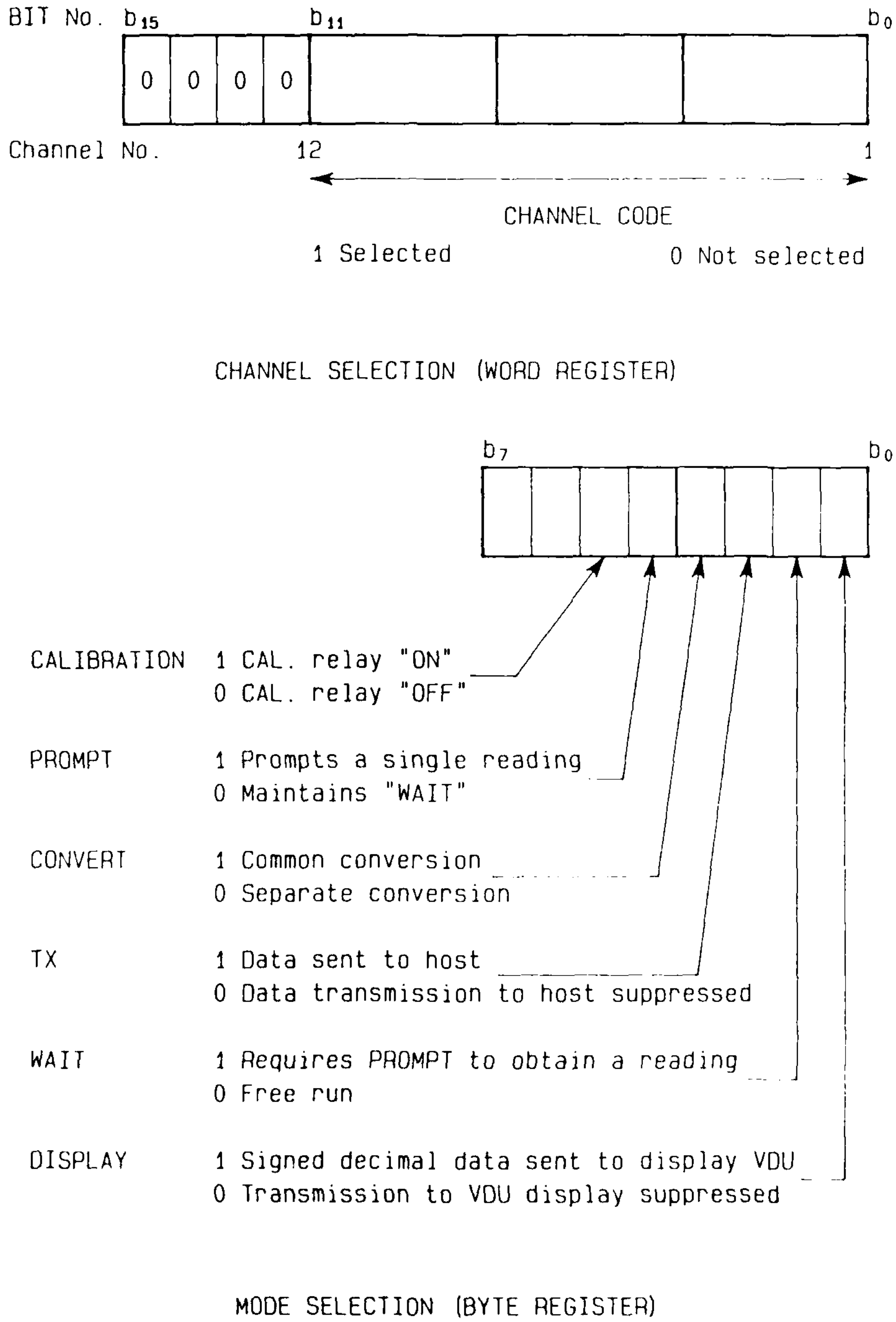


FIG. 14 BIT FUNCTIONS IN CONTROL BLOCK

CHANNEL SELECTION

ASCII CHAR TO SELECT A BLOCK OF 4 CHANNEL NUMBERS

M.S. 60	50	40	12 / 8 / 4	11 / 7 / 3	10 / 6 / 2	9 / 5 / 1	LS
`	P	@					0000
a	Q	A				✓	0001
b	R	B			✓		0010
c	S	C			✓	✓	0011
d	T	D		✓			0100
e	U	E		✓		✓	0101
f	V	F		✓	✓		0110
g	W	G		✓	✓	✓	0111
h	X	H	✓				1000
i	Y	I	✓			✓	1001
j	Z	J	✓		✓		1010
k	[	K	✓		✓	✓	1011
l	\	L	✓	✓			1100
m	]	M	✓	✓		✓	1101
n	^	N	✓	✓	✓		1110
o	_	O	✓	✓	✓	✓	1111

CHANNEL No'S

e.g. k selects channels 9, 10 and 12
K selects channels 1, 2 and 4

MODE CODES

USEFUL FUNCTIONS (WITH DATA SENT TO HOST)	ASCII CODE	ASCII CHAR	
FREE RUN (WITHOUT DECIMAL DISPLAY)	2C	,	WITHOUT SCALED VOLTAGE DISPLAY TO TERMINAL
HALT FREE RUN	2E	.	
PROMPTS A SINGLE READING	31	1	
FREE RUN (WITH DECIMAL DISPLAY)	2D	-	WITH SCALED VOLTAGE DISPLAY TO TERMINAL
HALT FREE RUN	28	(	
ARMS FOR PROMPT (INITIATES A READING)	2F	/	
PROMPTS A SINGLE READING	31	1	
PROMPTS A SINGLE "CAL" READING	33	3	

CHARACTER BYTE FROM HOST →

	b_6	b_5	b_4	b_3	b_2	b_1	b_0

CONTAINS 4 BIT REPLACEMENT CODE (b_3–b_0)

b_6	b_5	b_4	
0	1	0	LOWER HALF OF MODE CODE
0	1	1	UPPER HALF OF MODE CODE
1	0	0	LOW BLOCK OF CHANNEL SELECTION CODE
1	0	1	MID BLOCK OF CHANNEL SELECTION CODE
1	0	0	HIGH BLOCK OF CHANNEL SELECTION CODE
1	0	1	NOT ASSIGNED

PORT	USE	NON SELECTED	MISSING	OVERLOAD	EXCITATION	TIMED OUT	DATA	CALIBRATE
UPPER LOWER	TERMINAL HOST	SPACES SPACES	???? ????	MESSAGE "$" LEADS 0/4 CHANNEL DATA	MESSAGE "SGLO" LEADS DATA STRING	MESSAGE "TIMEOUT"	SCALED VOLTAGE HEX VALUES (ASCII CODED)	MESSAGE "STD" LEADS DATA STRING

FIG. 15 SUMMARY OF HOST COMMAND CODES FOR S.G.C. MODULE

FIG. 16 OPTO ISOLATOR CARD

BIT No.

b_{15} ... b_0

EXC	PAR & MON	SER & PAR	N/C	12	11	10	9	8	7	6	5	4	3	2	1

S/W STATE

CHANNEL No.

(bit state "1" represents channel "OVERLOAD" error)

b_{14}	b_{13}	SWITCH SELECTION
1	0	PARALLEL COMMUNICATION WITH HOST
0	1	SERIAL
1	1	PARALLEL

b_{15} state "1" rerpesents A.C. excitation level "LOW" error

FIG. 17 OPTO ISOLATOR STATUS REGISTER BIT FUNCTIONS

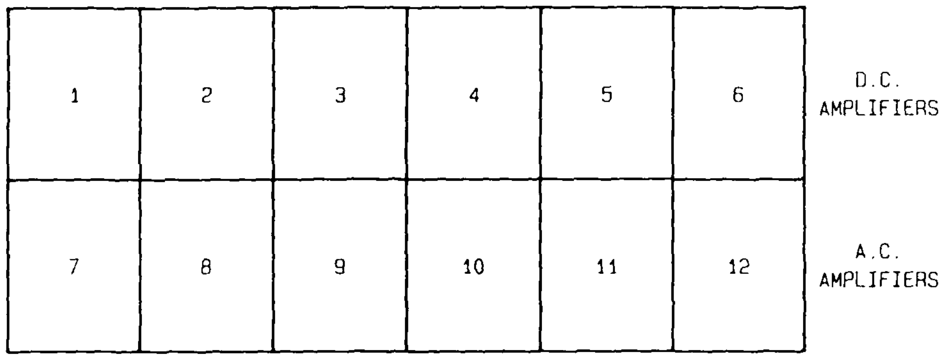


FIG. 18(a) AMPLIFIER CHANNEL ALLOCATION (FRONT VIEW)

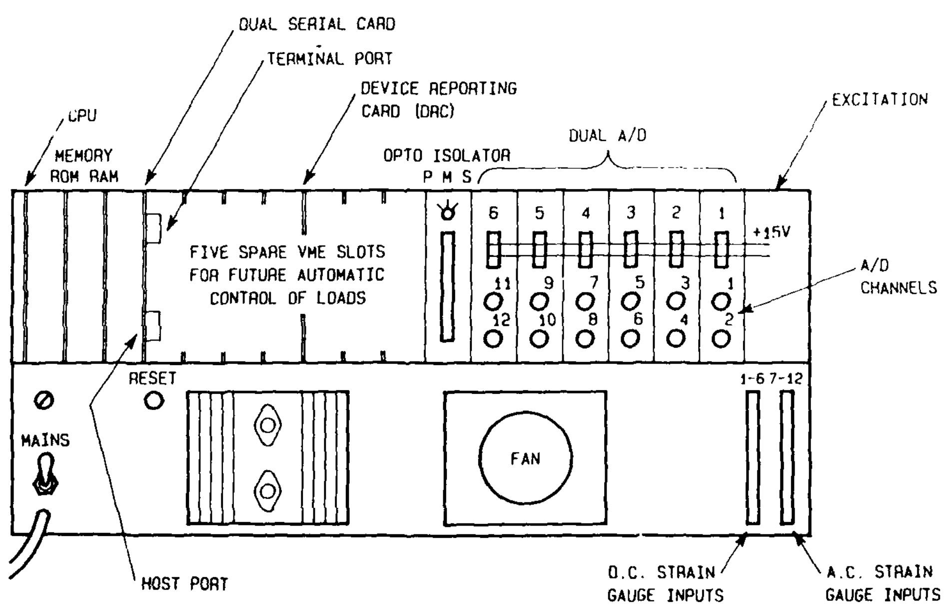


FIG. 18(b) MICROPROCESSOR CARDS AND CONNECTOR IDENTIFICATION
(REAR VIEW)

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